Advanced

GT34TS04A

Temperature Sensor

With 4K Bits

SPD EEPROM

Table of Contents

1. Features

- Supply voltage:1.7V to 3.6V (SPD EEPROM) and 2.2V to 3.6V(TS)
- JEDEC TSE2004av Compliant Temperature Sensor
- 2-wire serial interface I²C/SMBus compatible
- Low operating current
  - 5 μA (max) TS in Shutdown mode and EEPROM in Standby mode
  - 500 μA (max) TS being active and EEPROM in Standby mode
  - 2 mA (max) TS in Shutdown mode and EEPROM is in Active mode.
- Software Programmable Shutdown Mode
- Software reset feature
- Speed up to 1 MHz in I²C bus (Fast Mode) and 100KHz in SMBus 2.0

1.1 The 4Kb SPD EEPROM Features

- Functionality identical to SPD EEPROM
- Byte and Page Write Operations
  - Page Size up to 16 bytes
- Random and Sequential Read modes
- Self-Time Write Cycle (5ms, max)
- Automatic Address Incrementing
- Individual Reversible Software data Protection for all the four 128 byte blocks
- Noise filter on bus inputs
- More than 1 million Erase/Write Endurance Cycles
- More than 40 years Data Retention
- Operating Temperature range: -40°C to +85°C

1.2 Temperature Sensor Features

- Temperature sensor accuracy:
  - ±0.5°C(Typ.) from +70°C to +95°C
  - ±1°C(Typ.) from +40°C to +125°C
  - ±2°C(Typ.) from -40°C to +125°C
- Temperature sensor resolution: 0.25°C/LSB (default)
- The TS continuously monitors the temperature and updates the temperature data typically eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.
- Temperature sampling (ADC conversion) time: 125 msec (max.)
- Hysteresis selectable set points from: 0, 1.5°C, 3°C & 6°C
- Ambient temperature sensing range: -40°C to +125°C

2. General Description

The GT34TS04A is a Temperature Sensor (TS) product with embedded 4K-bit Serial Presence Detect (SPD) EEPROM, which is fully compatible to industrial standard I²C/SMBus interface and compliant to the JEDEC 42.4 specification. The EEPROM memory is organized as two pages of 256 bytes each or 512 bytes of total memory. Each page is comprised of two 128-byte blocks. The devices are able to selectively lock the data in any or all of the four 128-byte blocks. This product is designed for memory module applications in most PC and Server platforms, as well as other related applications. All the information concerning the DRAM module configuration (such as its access speed, its size, and its organization) can be kept write protected in one or more of the blocks of memory.

The unique GT34TS04A product operates from 1.7V to 3.6V and is offered in 8-pin Ultra-thin DFN package, 2 mm x 3 mm x 0.6 mm (max.), which is lead-free, RoHS, halogen free or Green compliance, providing space as well as cost saving for DIMM manufactures.

2.1 4K-bit SPD EEPROM

The embedded 4K-bit serial SPD EEPROM are protocol compatible with previous generation 2Kbit device such as GT34C02A or GT34TS02. The page selection method allows commands used with legacy device such as GT34C02A or GT34TS02 to applied to the lower or upper pages of the EE/Temperature Sensor. In this way, the GT34TS04A may be used in legacy applications without software changes. Minor exceptions to this compatibility, such as elimination of the Permanent write Protect feature, are documented. Individually locking a 128-byte block of the EEPROM may be accomplished using a software write protection mechanism in conjunction with a high input voltage V_{HV} on input SA0. By sending the device a specific I²C Bus sequence, each block may be protected from writes until write protection is electrically reversed using a separate I²C Bus sequence which also requires V_{HV} on input SA0. Write protection for all four blocks is cleared simultaneously, and write protection may be re-asserted after being cleared. The operating ambient temperature ranging is from -40°C to +85°C.

2.2 Temperature Sensor

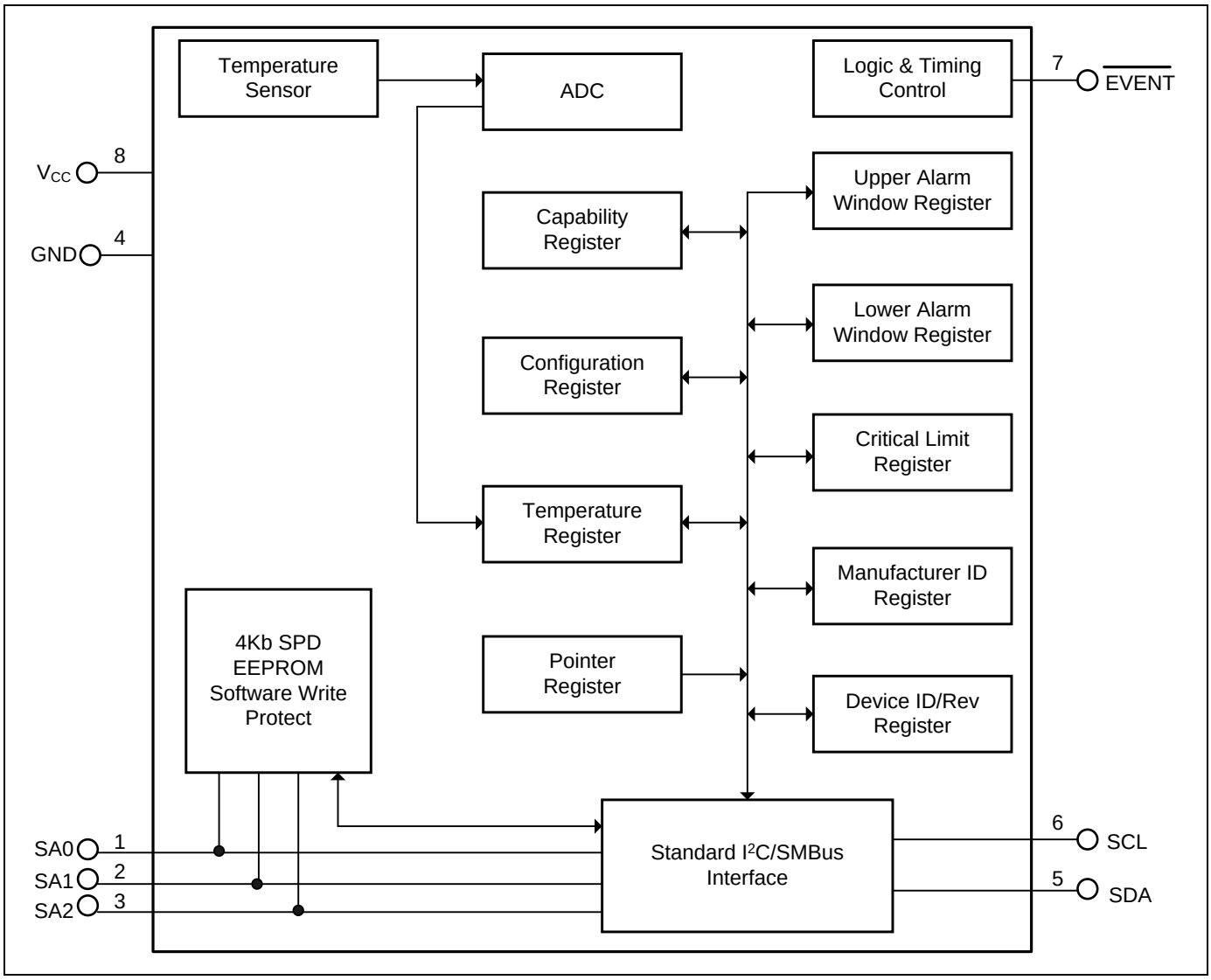
The TS monitors the ambient temperature ranging from -40°C to 125°C. The TS includes a high precision CMOS temperature sensor, a sigma-delta analog to digital converter (ADC) and a serial interface compatible to industrial standard I²C/SMBus. The ADC default resolution is set at 10-bit (0.25°C). The accuracy over various temperature ranges is:

- ±0.5°C (Typ.) for temperature range from +70°C to +95°C
- ±1°C (Typ.) for temperature range from +40°C to +125°
- ±2°C (Typ.) for temperature range from -40°C to 125°C

The TS has shutdown current 100 μA (max.) with SPD EE in Standby mode.

The TS component has user-programmable registers that are used to configure both the TS performance and response to over-temperature conditions. The device contains programmable high, low and critical temperature limits. Finally, the device **$\overline{\text{EVENT}}$** pin can be configured as active high or active low and can be configured to operate as an interrupt or as a comparator output.

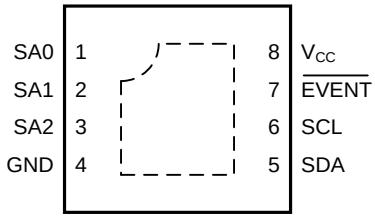
3. Functional Block Diagram



4. Pin Configuration

4.1 8-Lead UDFN

Top View



4.2 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	SA0	I	Device Address Input
2	SA1	I	Device Address Input
3	SA2	I	Device Address Input
4	GND	-	Ground
5	SDA	I/O	Serial Address, Data input and Data output (Open drain)
6	SCL	I	Serial Clock Input
7	$\overline{\text{EVENT}}$	O	Temperature Event Pin
8	V_{CC}	-	Power Supply

Note: Thermal sensing devices also have a heat paddle, typically connected to the application ground plane.

4.3 Pin Descriptions

SCL

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{CC}. (Figure 4.1 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

SDA

The bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signal on the bus. A pull up resistor must be connected from Serial Data (SDA) to the most positive V_{CC} in the I^2C Bus chain. (Figure 4.1 indicates how the value of the pull-up resistor can be calculated).

SA0, SA1, SA2

These input signals are used to create the Logical Serial Address LSA that is compared to the three least significant bits(b3, b2, b1) of the 7-bit Slave Address.(Pls refer to table 5.1 for details on LSA encoding).

The SA0 input is also used to detect the V_{HV} voltage when decoding a SWPn or CWP instruction. (Pls refer to table5.1

for decode details).

$\overline{\text{EVENT}}$

The **$\overline{\text{EVENT}}$** pin is an open-drain pin that requires a pull-up to V_{CC} on the system motherboard or integrated into the master controller. **$\overline{\text{EVENT}}$** has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt, Comparator, or TCRIT Only.

In Interrupt Mode the **$\overline{\text{EVENT}}$** pin will remain asserted until it is released by writing a '1' to the "Clear Event" bit in the Status Register. The value to write is independent of the **$\overline{\text{EVENT}}$** polarity bit.

In Comparator Mode the **$\overline{\text{EVENT}}$** pin will clear itself when the error condition that caused the pin to be asserted is removed. When the temperature is compared against the TCRIT limit, then this mode is always used.

Finally, in the TCRIT Only Mode the **$\overline{\text{EVENT}}$** pin will only be asserted if the measured temperature exceeds the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus the TCRIT hysteresis. Figure 7.5 illustrates the operation of the different modes over time and temperature.

The systems that use the active high mode for **$\overline{\text{EVENT}}$** must be wired point to point between the GT34TS04A and the sensing controller. Wire-OR configurations should not be used with active high **$\overline{\text{EVENT}}$** since any device pulling the **$\overline{\text{EVENT}}$** signal low will mask the other devices on the bus. Also note that the normal state of **$\overline{\text{EVENT}}$** in active high mode is a '0' which will constantly draw power through the pull-up resistor.

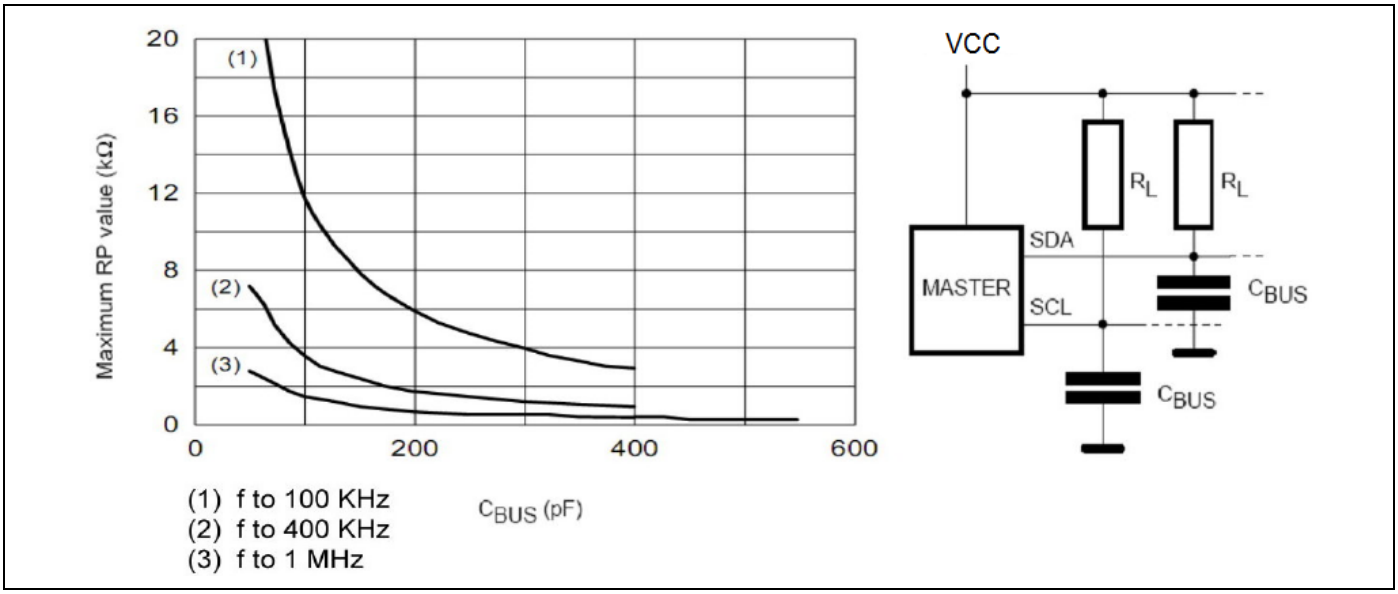
V_{CC}

Supply voltage.

GND

Ground of supply voltage.

Figure 4.1 Maximum RL Value Versus Bus Capacitance (CBUS) for an I²C Bus



5. I²C / SMBus Serial Interface

5.1 Serial bus interface

The GT34TS04A behaves as a slave device in the I²C Bus protocol, with all operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and R/$\overline{W}$ bit (as described in Table5.1), terminated by an acknowledge bit. GT34TS04A shall not initiate clock stretching, which is an optional I²C Bus feature.

In accordance with the I²C Bus definition, the GT34TS04A use three (3) built-in, 4-bit Device Type Identifier Codes (DTIC) and a 3-bit Select Address to generate an I²C Bus Slave Address.

The EE memory may be accessed using a DTIC of (1010), and to perform the SWPn, RSPn, or CWP operations a DTIC of (0110) is required. The TS registers of the GT34TS04A are accessed using a DTIC of (0011).

EE and TS portions of this device are designed to operate in parallel. Accesses to each portion of the device may be interleaved as long as the command protocol is followed.

5.2 I²C / SMBus Communication

When writing data to the memory, an acknowledge bit is inserted during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Bus Master generated STOP condition after an Ack for WRITE, and after a NoAck for READ. Violations of the command protocol result in unpredictable operation.

The TS section of the GT34TS04A uses a pointer register to access all registers in the device. Additionally, all data transfers to and from this section of the device are performed as block read/write operations. The data is transmitted/received as 2 bytes, Most Significant Byte (MSB) first, and terminated with a NoAck and STOP after the Least Significant byte (LSB). Data and address information is transmitted and received Most Significant Bit first.

5.3 Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

5.4 Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master.

A Read command that is followed by NoAck can be followed by a Stop condition to force the EE into Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle for the EE. Neither of these conditions changes the operation of the TS section of a GT34TS04A.

5.5 Acknowledge

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it is bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits. The no-acknowledge bit is used to indicate the completion of a block read operation, or an attempt to modify a write-protected register. The bus master releases Serial Data (SDA) after sending eight bits of data, and during the 9th clock pulse period, and does not pull Serial Data (SDA) Low.

5.6 Slave address

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 5.2 (on Serial Data (SDA), most significant bit first). The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Select Address. To address the EE memory array, the 4-bit Device Type Identifier is 1010b; to access the write protection settings or

EE page address, it is 0110b; and to access the Temperature Sensor settings is 0011b. Additionally, writing or clearing the reversible EE write protect requires that SA0 be raised to the V_{HV} voltage level.

Up to eight devices can be connected on a single I^2C Bus. Each one is given a unique 3-bit Logical Serial Address code. The LSA is a decoding of information on the SA pins SA0, SA1, and SA2 as described in Table 5.2. When the Device Select Code is received, the device only responds if the Select Address is the same as the Logical Serial Address. Write Protection commands SWPn, CWP, and RPSn, and the EE Page Address commands SPAn and RPA, do not use the Select Address or Logical Serial Address, therefore all devices on the I^2C Bus will act on these commands simultaneously. Since it is impossible to determine which device is responding to RPSn or RPA commands, for example, these functions are primarily used for external device programmers rather than in-system applications.

The 8^{th} bit is the Read/Write bit (R/$\overline{W}$). This bit is set to 1 for Read and 0 for Write operations. If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9^{th} bit time. If the device does not match the Device Select code, the EE section deselects itself from the bus, and goes into Standby mode. The I^2C Bus operating modes are detailed in Table 5.1.

5.7 Power-Up and Reset States

5. 7.1 Power-Up Condition

In order to prevent inadvertent operations during power up, a Power On Reset (POR) circuit is included. On cold power on, V_{CC} must rise monotonically between V_{PON} and V_{CC}(min) without ringback to ensure proper startup. Once V_{CC} has passed the V_{PON} threshold, the device is reset.

Prior to selecting the memory and issuing instructions, a valid and stable V_{CC} voltage must be applied, and no command may be issued to the device for T_{INIT}. The supply voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (T_W).

At power down (phase during which V_{CC} decreases continuously), as soon as V_{CC} drops from the normal operating voltage below the minimum operating voltage, the device stops responding to commands. On warm power cycling, V_{CC} must remain below V_{POFF} for T_{POFF}, and must meet cold power on reset timing when restoring power.

The devices are delivered with all bits in the EEPROM memory array set to '1' (each byte contains 0xFF).

5. 7.2 Software Reset

The GT34TS04A has three software commands for setting, clearing, or interrogating the write-protection status.

- SWPn: Set Write Protection for Block n
- CWP: Clear Write Protection for all blocks
- RPSn: Read Protection Status for Block n

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 0
- Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 1
- Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 1

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

Table 5.1 I²C Bus Operating Mode

Mode	R/$\overline{W}$ Bit	Bytes	Initial Sequence
EEPROM Current Address Read	1	1	START, Device Select, R/$\overline{W}$ =1
EEPROM Random Address Read	0	1	START, Device Select, R/$\overline{W}$ =0, Address
	1		reSTART, Device Select, R/$\overline{W}$ =1
EEPROM Sequential Read	1	≥1	Similar to Current or Random Address Read
EEPROM Byte Write	0	1	START, Device Select, R/$\overline{W}$ =0, Data, STOP
EEPROM Page Write	0	≤16	START, Device Select, R/$\overline{W}$ =0, Data, STOP
TS Write	0	2	START, Device Select, R/$\overline{W}$ =0, Pointer, Data, STOP
TS Read	1	2	START, Device Select, R/$\overline{W}$ =1, Pointer, Data, STOP

Table 5.2 Device Select Code

Function	Abbr	Device Type Identifier[1]				Select Address[2,4]			R/$\overline{W}$	SA0 Pin[3]
		B7	B6	B5	B4	B3	B2	B1		
Read Temperature Register[8]	RTR	0	0	1	1	LSA2	LSA1	LSA0	1	0 or 1
Write Temperature Register[8]	WTR								0	
Read EE Memory	RSPD	1	0	1	0	LSA2	LSA1	LSA0	1	0 or 1
Write EE Memory	WSPD								0	
Set Write Protection, Block0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, Block1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, Block2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, Block3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, Block0	RPS0					0	0	1	1	0,1, or V_{HV}
Read Protection Status, Block1	RPS1					1	0	0	1	0,1, or V_{HV}
Read Protection Status, Block2	RPS2					1	0	1	1	0,1, or V_{HV}
Read Protection Status, Block3	RPS3					0	0	0	1	0,1, or V_{HV}
Set EE Page Address to 0[5]	SPA0					1	1	0	0	0,1, or V_{HV}
Set EE Page Address to 1[5]	SPA1					1	1	1	0	0,1, or V_{HV}
Read EE Page Address to 0[6]	RPA					1	1	0	1	0,1, or V_{HV}
Reserved	--					All Other Encodings				

Note: [1] The most significant bit, b7, is sent first.

[2] Logical Serial Addresses (LSA) are generated by the combination of inputs on the SA pins

[3] SA0 pin is driven to 0 = GND, 1 = V_{CC}, or V_{HV}

[4] For backward compatibility with previous devices, the order of block select bits (b3 and b1) are not a simple binary encoding of the block number.

[5] Set EE page address to 0 selects the lower 256 bytes of EEPROM, setting to 1 selects the upper 256 bytes of EEPROM. Subsequent Read EE or Write EE commands operate on the selected EE page.

[6] Reading the EE page address results in Ack when the current page is 0 and NoAck when the current page is 1.

[7] Permanent Write Protect features have been eliminated from the devices.

[8] GT34TS04A Only

Figure 5.1 V_{CC} Ramp Up and Ramp Down

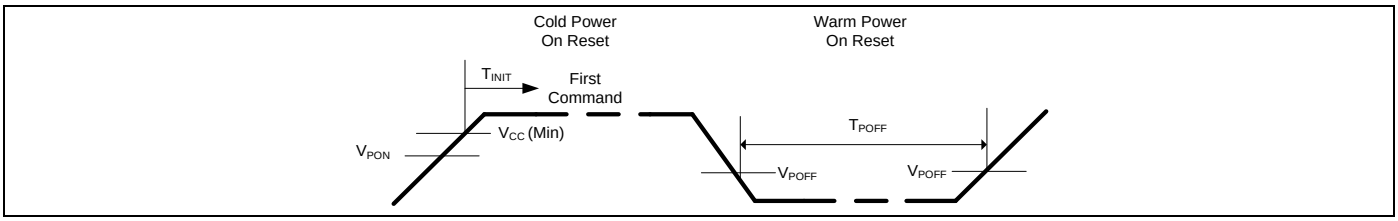


Figure 5.2. Typical System Bus Configuration

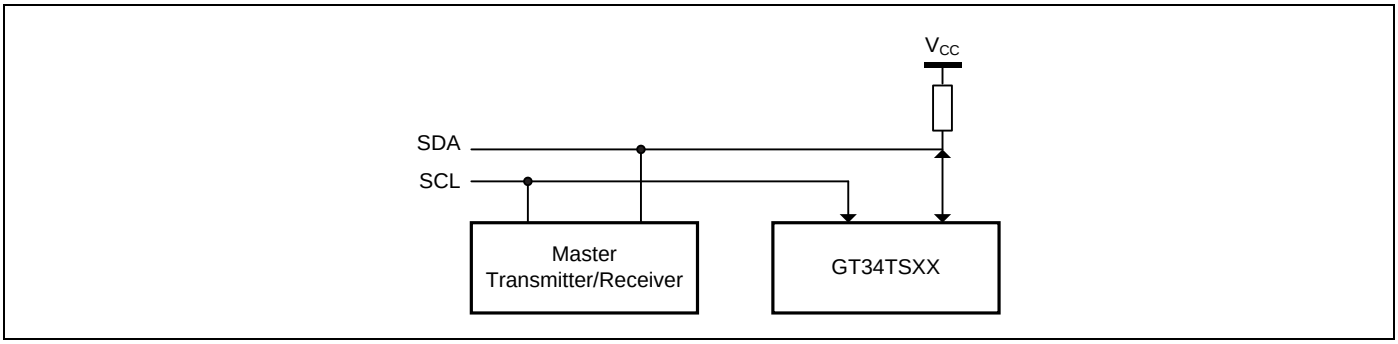


Figure 5.3. Start and Stop Conditions

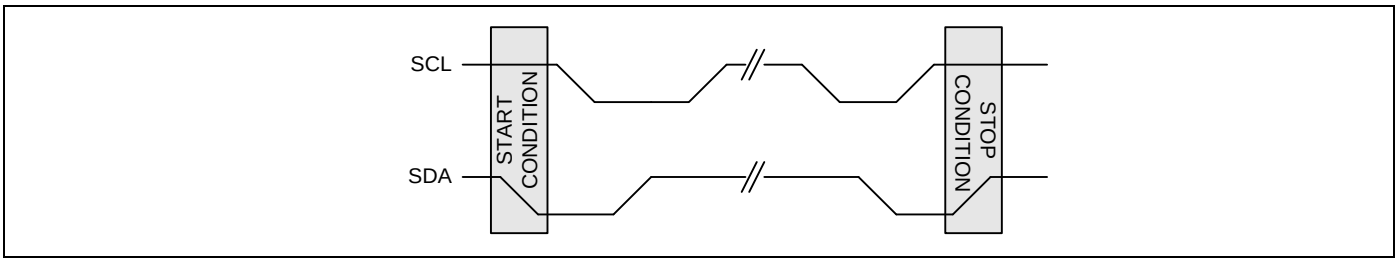


Figure 5.4. Data Validity Protocol

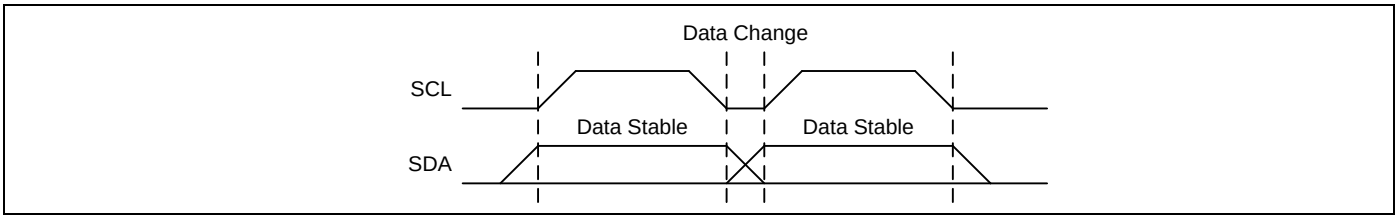


Figure 5.5. Output Acknowledge

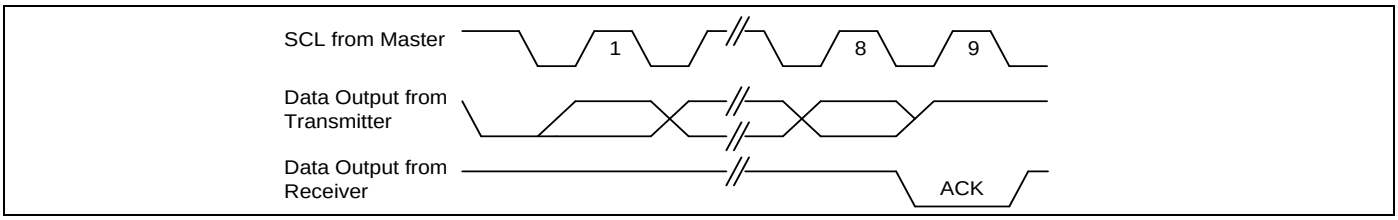


Figure 5.6. Bus Timing

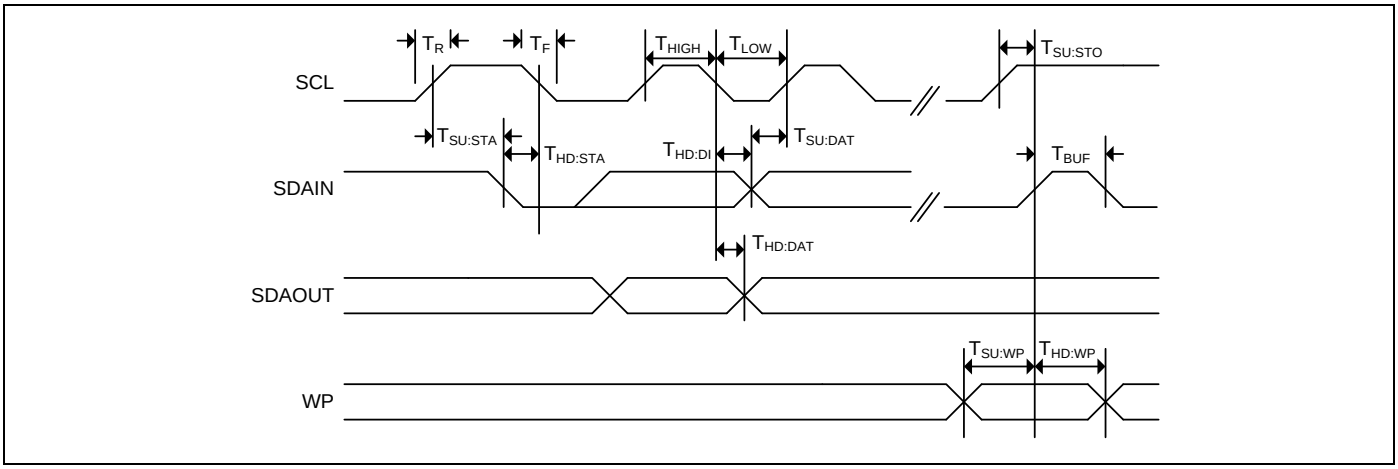


Figure 5.7. Write Cycle Timing

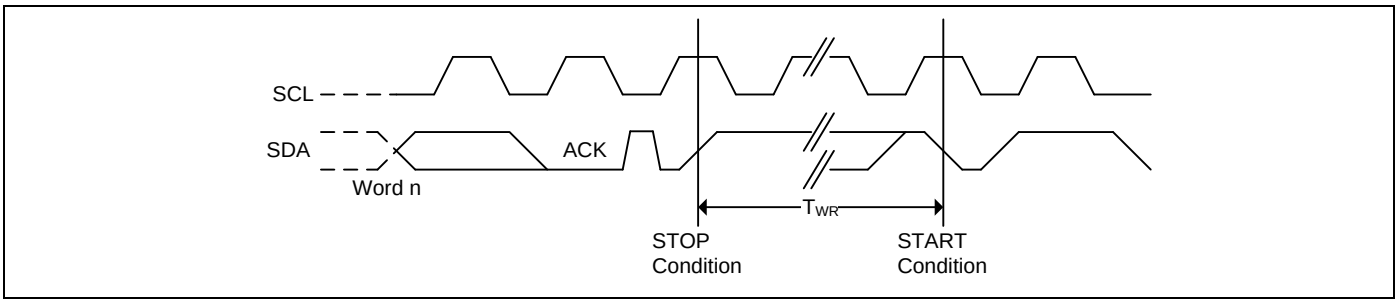
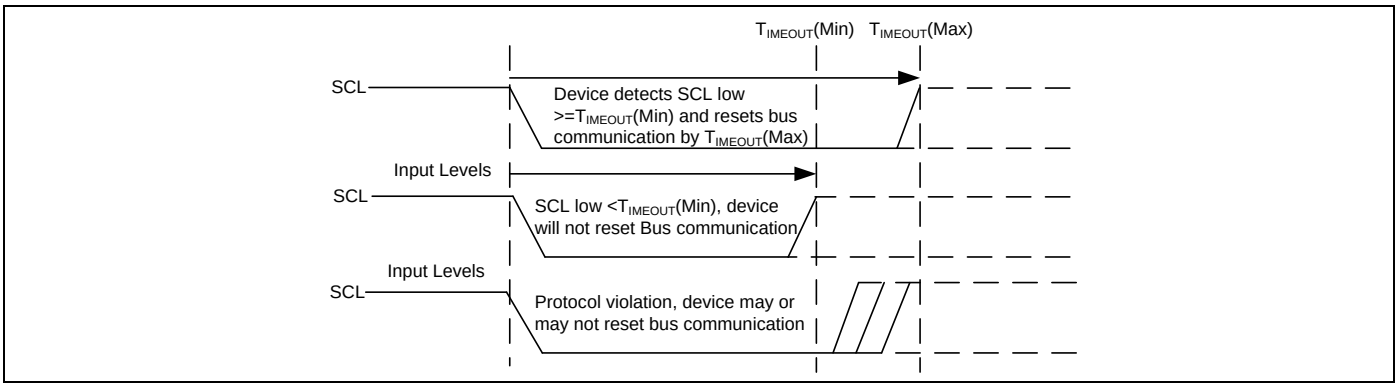


Figure 5.8. Bus Timeout Waveform



6. EEPROM Functional Description

6.1 Write Operation

Following a Start condition the bus master sends a Device Select Code with the R/$\overline{W}$ bit reset to 0. The device acknowledges this, as shown in Figure 6.1 and 6.2, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored by the EE, and the EE device does not respond to any requests. For GT34TS04A, access to the TS portion of the device is permitted during this period.

The device has an internal address counter which is incremented each time a byte is written. If a Write operation is performed to a protected block, the internal address counter is not incremented.

6.1.1 Byte Write

After the Device Select Code and the address byte, the bus master sends one data byte. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. After the byte is transferred, the internal byte address counter is incremented unless the block is write protected. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 6.1.

6.1.2 Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as "roll-over' occurs. This should be avoided, as data starts to be over-written in an implementation dependent fashion.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter is incremented unless the block is write-protected. The transfer is terminated by the bus master generating a Stop condition, as shown in Figure 6.2.

6.1.3 Write Cycle Polling Using ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (T_W) is shown in AC Electric characteristic table, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 6.8, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, NoAck will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

6.2 Read Operation

Read operations are performed independent of the software protection state.

The device has an internal address counter which is incremented each time a byte is read.

6.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in Figure 6.3) but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code,

with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition.

6.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 6.4, without acknowledging the byte.

6.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition, as shown in Figure 6.5.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 0x00.

6.2.4 Acknowledge In Read Mode

For all Read commands to the SPD, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and returns to an idle state to await the next valid START condition. This has no effect on the TS operational status, as shown in Table 6.2.

6.3 Write Protection

6.3.1 Software Write Protection

The devices have three software commands for setting, clearing, or interrogating the write-protection status.

- SWPn: Set Write Protection for Block n
- CWP: Clear Write Protection for all blocks
- RPSn: Read Protection Status for Block n

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 0
- Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 1
- Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 1

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

6.3.2 Set and Clear Write Protection

If the software write-protection has been set with the SWPn instruction, it may be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears write protection for all blocks, as shown in Figure 6.6 and Table 6.1.

6.3.3 Read Protection Status

The controller issues a RPSn command specifying which block to report upon. If Software Write Protection has not been set, the device replies to the data byte with an Ack. If Software Write Protection has been set, the device replies to the data byte with a NoAck, as shown in Figure 6.7 and Table 6.2.

6.3.4 Read SPD Page Address

The controller issues an RPA command to determine if the currently selected SPD page is 0 (device returns Ack) or 1 (device returns NoAck).

6.3.5 Set SPD Page Address

The controller issues an SPAn command to select the lower 256 bytes (SPA0) or upper 256 bytes (SPA1) as shown in figure 6.6. After a cold or warm power-on reset, the SPD Page Address is always 0, selecting the lower 256 bytes.

Figure 6.1 Byte Write

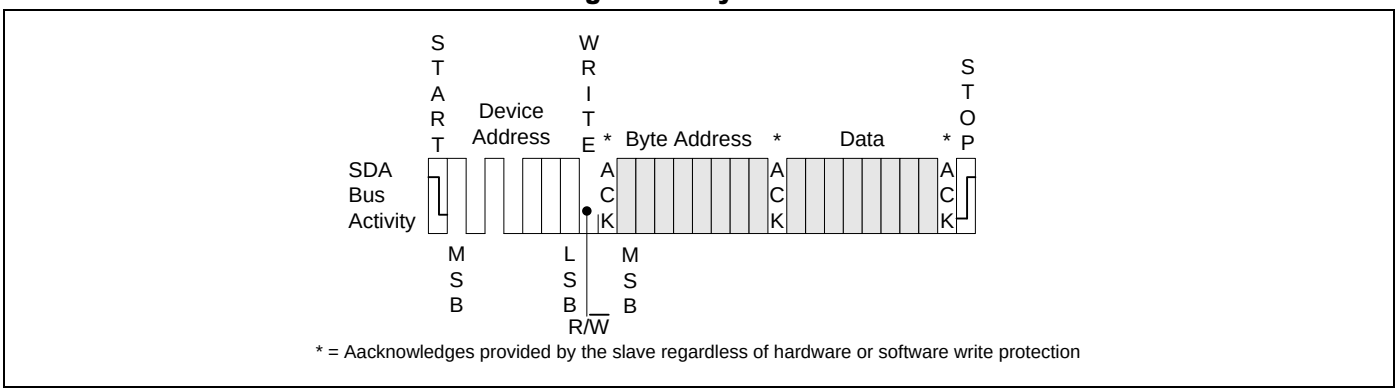


Figure 6.2 Page Write

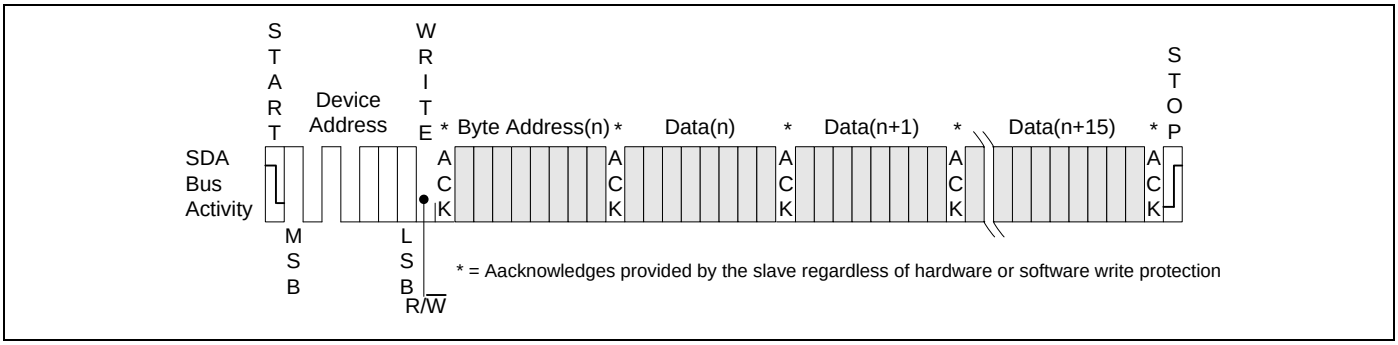


Figure 6.3 Random Address Read

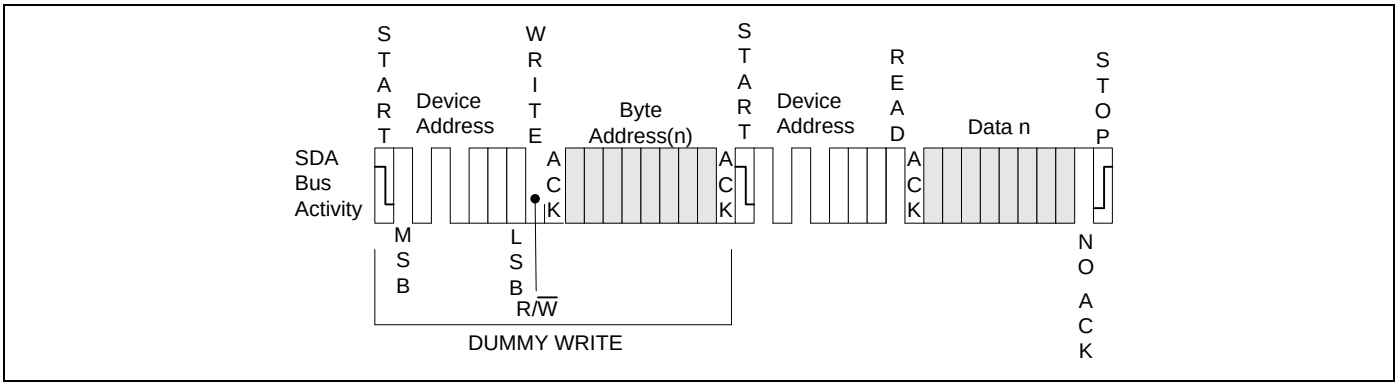


Figure 6.4 Current Address Read

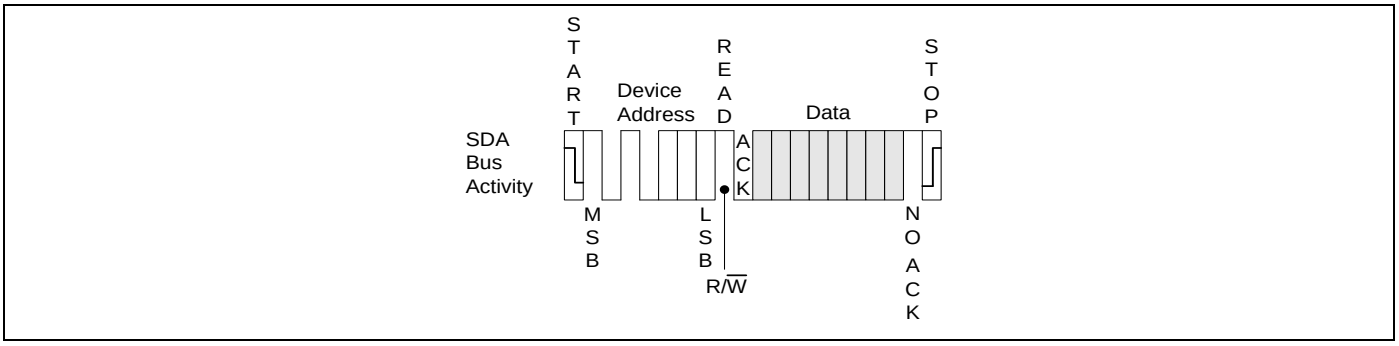


Figure 6.5 Sequential Read

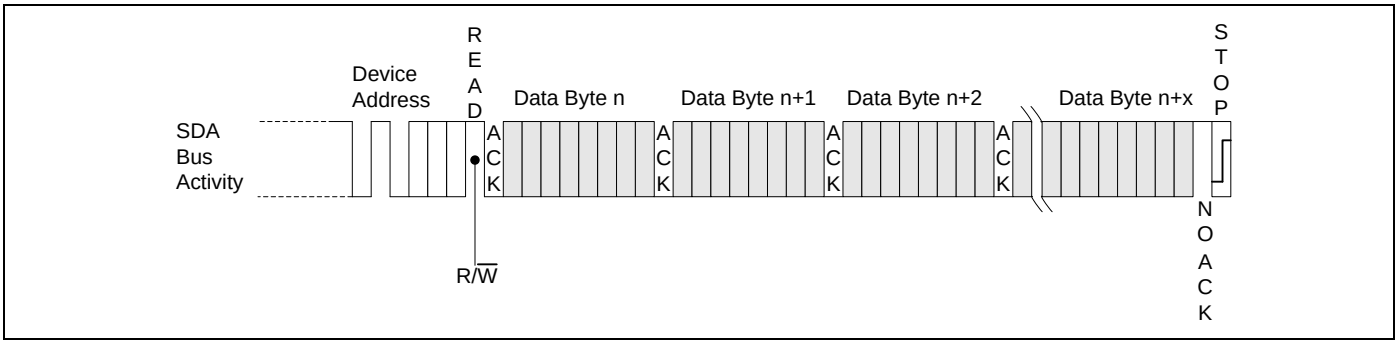


Figure 6.6 Set and Clear Write Protection; Set Page Address

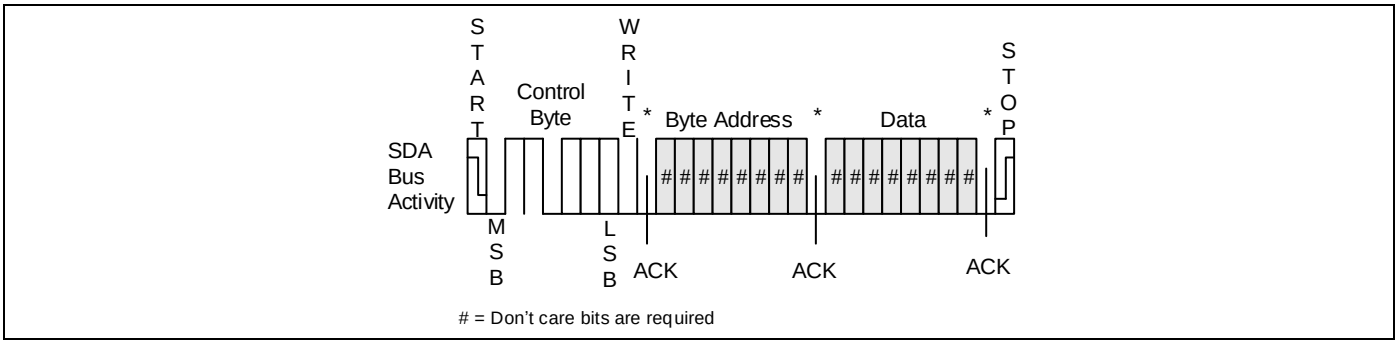


Figure 6.7 Read Write Protection Status; Read Page Address

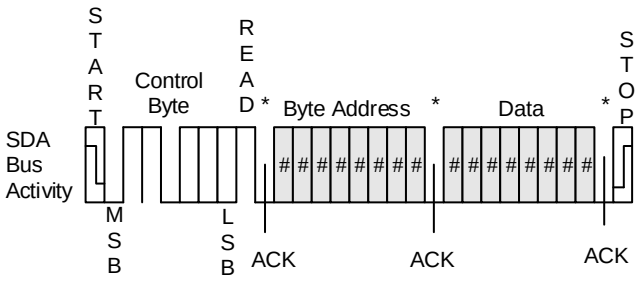

START
Control Byte
READ
*
Byte Address
*
Data
*
STOP
SDA Bus Activity
MSB
LSB
ACK
ACK
ACK
= Don't care bits are required

Figure 6.8 Write Cycle Polling Flowchart for EE using ACK

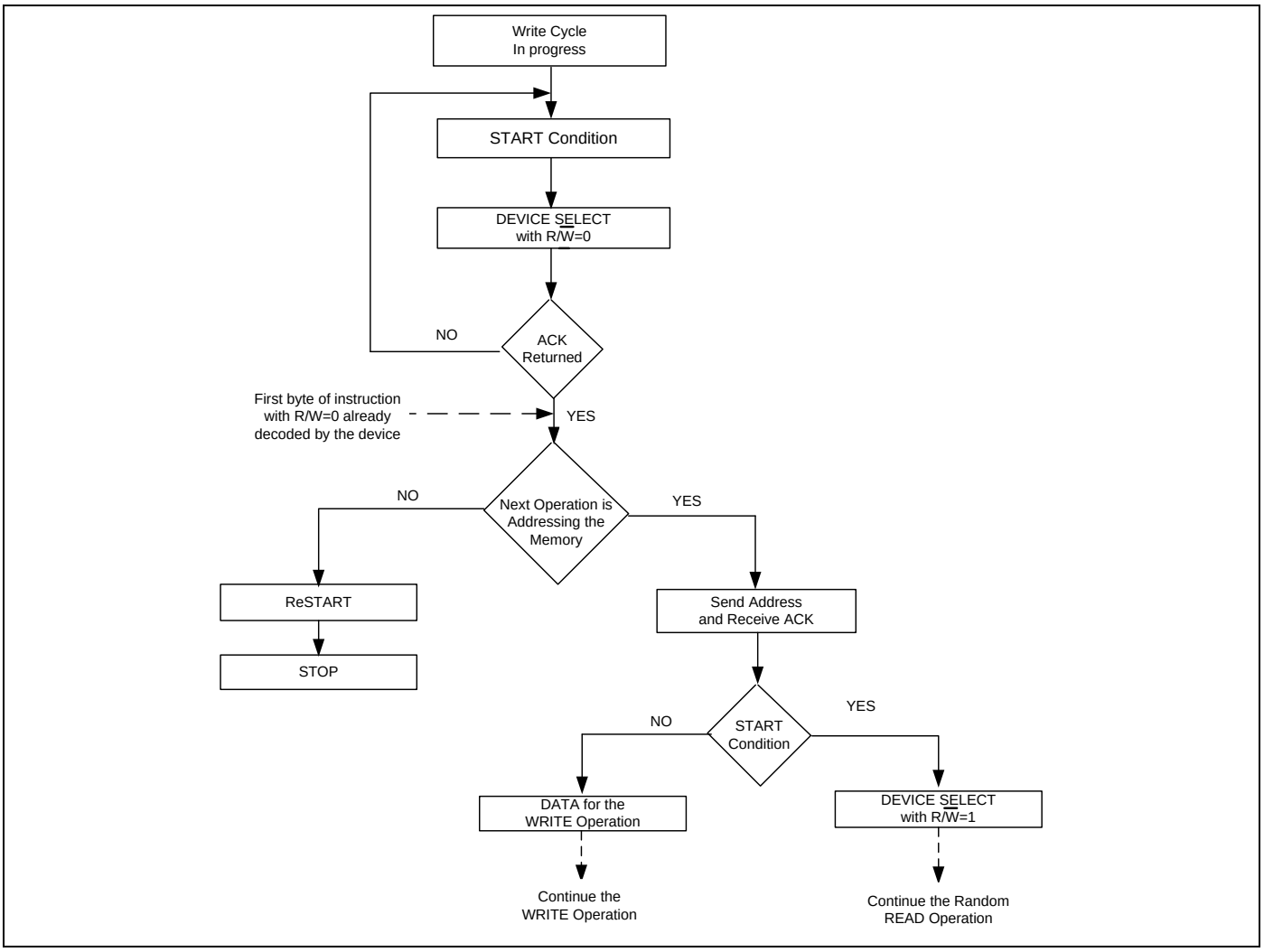


Table 6.1 Acknowledge When Writing Data or Defining Write Protection

Status	Instruction	ACK	Address	ACK	Data Byte	ACK	Write Cycle (T_W)
Protected with SWPn	SWPn	NoACK	Not signaificant	NoACK	Not signaificant	NoACK	No
	CWP	ACK	Not signaificant	ACK	Not signaificant	ACK	Yes
	Page or byte write in protected block	ACK	Address	ACK	Data	NoACK	No
Not Protected	SWPn or CWP	ACK	Not signaificant	ACK	Not signaificant	ACK	Yes
	Page or byte write	ACK	Address	ACK	Data	ACK	Yes

Table 6.2 Acknowledge When Reading the Protection Status

SWPn Status	Instruction	ACK	Address	ACK	Data Byte	ACK
Set	RPSn	NoACK	Not signaificant	NoACK	Not signaificant	NoACK
Not Set	RPSn	ACK	Not signaificant	NoACK	Not signaificant	NoACK

7. Temperature Sensor

7.1 TS Register Overview

The GT34TS04A Temperature Register Set is accessed though the I²C Bus address 0011_bbb_ R/$\overline{W}$. The "bbb" denotes the Logical Serial Address code LSA. In the event SA0 is in the high voltage state, the device shall not recognize the LSA. The Temperature Register Set stores the temperature data, limits, and configuration values. All registers in the address space from 0x00 through 0x08 are 16-bit registers, accessed through block read and write commands.

Behavior on accesses to invalid register locations is vendor-specific and may return an Ack or a NoAck.

7.2 TS Write Operation

Writing to the GT34TS04A Temperature Register Set is accomplished through a modified block write operation for two (2) data bytes. To maintain I²C Bus compatibility, the 16 bit register is accessed through a pointer register, requiring the write sequence to include an address pointer in addition to the Slave address. This indicates the storage location for the next two bytes received.

Figure 7.1 shows an entire write transaction on the bus.

7.3 TS Read Operation

Reading data from the TS may be accomplished in one of two ways:

1. If the location latched in the Pointer Register is correct (for normal operation it is expected the same address will be read repeatedly for temperature), the read sequence may consist of a Slave Address from the bus master followed by two bytes of data from the device; or
2. The pointer register is loaded with the correct register address, and the data is read. The sequence to preset the pointer register is shown in Figure 7.2, and the preset pointer read is shown in Figure 7.3. If it is desired to read random address each cycle, the complete Pointer Write, Word Read sequence is shown in Figure 7.4.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (Ack) or No Acknowledge (NoAck) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

7.4 TS Register Set Definition

The register set address is shown in Table 7.1. These values are used in the I²C Bus operations as the "REG_PTR" in Figures 7.1 to Figure 7.4.

Table 7.1 TS Register Summary

Address	R/$\overline{W}$	Name	Function	Default
N/A	W	Address Pointer	Address storage for subsequent operations	Undefined
00h	R	Capabilities	Indicates the functions and capabilities of the temperature sensor	00EF
01h	R/$\overline{W}$	Configuration	Controls the operation of the temperature monitor	0000
02h	R/$\overline{W}$	High Limit	Temperature High Limit	0000
03h	R/$\overline{W}$	Low Limit	Temperature Low Limit	0000
04h	R/$\overline{W}$	TCRIT Limit	Critical Temperature	0000
05h	R	Ambient Temperature	Current Ambient Temperature	N/A
06h	R	Manufacturer ID	PCI-SIG manufacturer ID	1C68
07h	R	Device/Revision	Device ID and Revision number	2202
08h	R/$\overline{W}$	SMBus Timeout	SMBus Timeout status	0000
09h	R/$\overline{W}$	Temperature Resolution	Selected Temperature Resolution	0001

7.5 TS Capability Register

The TS Capabilities Register indicates the supported features of the temperature sensor portion of the GT34TS04A. This register is read-only and writing to it will have no effect.

Bit15 - Bit8 -- RFU - Reserved for future use. These bits will always read '0'

Bit7 - EVSD -- **$\overline{\text{EVENT}}$** with Shutdown action. Must be 1.

'0' - Not used.

'1' - The **$\overline{\text{EVENT}}$** output is deasserted (not driven) when entering shutdown, and remains deasserted upon exit from shutdown until the next thermal sample is taken, or possibly sooner if **$\overline{\text{EVENT}}$** is programmed for comparator mode. In interrupt mode, **$\overline{\text{EVENT}}$** may or may not be asserted when exiting shutdown if a pending interrupt has not been cleared.

Bit6 - TMOUT -- Bus timeout period during normal operation. Must be 1.

'0' - Not used.

'1' - Parameter $T_{TIMEOUT}$ is supported within the range of 25 to 35 ms.

Bit5 -- V_{HV}

'0' - Not used.

'1' - Defined for compatibility with TS3000 devices; since all EE/TSE devices are required to support V_{HV}, this bit is always '1'.

Bit4 - Bit3 -- TRES[1:0] - Indicates the resolution of the temperature monitor as shown in Table 7.3. The TRES[1:0] Default value is 01.

Bit2 - RANGE -- Indicates the supported temperature range.

'0' - Not used.

'1' - The temperature monitor can read temperatures below 0 °C and sets the sign bit appropriately.

Bit1 - ACC -- Indicates the supported temperature accuracy.

'0' - Not used.

'1' - The temperature monitor has ±1 °C accuracy over the active range (75 °C to 95 °C) and 2°C accuracy over the monitoring range (40 °C to 125 °C)

Bit0 - EVENT -- Indicates whether the temperature monitor supports interrupt capabilities

'0' - Not used.

'1' - The device supports interrupt capabilities.

Table 7.2 TS Capability Register

ADDR	R/$\overline{\text{W}}$	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0
00	R	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
		EVSD	TMOUT	V_{HV}	TRES[1:0]		RANGE	ACC	EVENT

Table 7.3 TRES Bit Decode

TRES[1:0]		Temperature Resolution
1	0	
0	0	0.5°C (9-bit)
0	1	0.25°C (10-bit)
1	0	0.125°C (11-bit)
1	1	0.0625°C (12-bit)

7.6 TS Configuration Register

The TS Configuration Register holds the control and status bits of the **EVENT** pin as well as general hysteresis on all limits.

Bits15 - 11 -- RFU - Reserved for future use. These bits will always read '0' and writing to them will have no effect. For future compatibility, all RFU bits must be programmed as '0'.

Bits10 - 9 -- HYST[1:0] - Control the hysteresis that is applied to all limits as shown in Table 7.5. This hysteresis applies to all limits when the temperature is dropping below the threshold so that once the temperature is above a given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. Note that hysteresis is also applied to **EVENT** pin functionality. When either of the lock bits is set, these bits cannot be altered.

Bit8 - SHDN -- Shutdown. The thermal sensing device and A/D converter are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However it can be cleared at any time. When in shutdown mode, GT34TS04A still respond to commands normally, however bus timeout may or may not be supported in this mode.

'0' (default) - The thermal sensor is active and converting.

'1' - The thermal sensor is disabled and will not generate interrupts or update the temperature data.

Bit7 - TCRIT_LOCK -- Locks the TCRIT Limit Register from being updated.

'0' (default) - The TCRIT Limit Register can be updated normally.

'1' - The TCRIT Limit Register is locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.

Bit6 - EVENT_LOCK -- Locks the High and Low Limit Registers from being updated.

'0' (default) - The High and Low Limit Registers can be updated normally.

'1' - The High and Low Limit Registers are locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.

Bit5 - CLEAR -- Clears the **EVENT** pin when it has been asserted. This bit is write-only and will always read '0'.

'0' - does nothing

'1' - The **EVENT** pin is released and will not be asserted until a new interrupt condition occurs. This bit is ignored if the device is operating in Comparator Mode. This bit is self clearing.

Bit4 - EVENT_STS -- Indicates if the **EVENT** pin is asserted. This bit is read only.

'0' (default) - The **EVENT** pin is not being asserted by the device.

'1' - The **EVENT** pin is being asserted by the device.

Bit3 - EVENT_CTRL -- Masks the **EVENT** pin from generating an interrupt. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

'0' (default) - The **EVENT** pin is disabled and will not generate interrupts.

'1' - The **EVENT** pin is enabled.

Bit2 - TCRIT_ONLY -- Controls whether the **EVENT** pin will be asserted from a high/low out-of-limit condition. When the EVENT_LOCK bit is set, this bit cannot be altered.

'0' (default) - The **EVENT** pin will be asserted if the measured temperature is above the High Limit or below the Low Limit in addition to if the temperature is above the TCRIT Limit.

'1' - The **EVENT** pin will only be asserted if the measured temperature is above the TCRIT Limit.

Bit1 - EVENT_POL -- Controls the "active" state of the **EVENT** pin. The **EVENT** pin is driven to this state when it is asserted. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

'0' (default) - The **EVENT** pin is active low. The "active" state of the pin will be logical '0'.

'1' - The **EVENT** pin is active high. The "active" state of the pin will be logical '1'.

Bit0 - EVENT_MODE -- Controls the behavior of the **EVENT** pin. The **EVENT** pin may function in either comparator or interrupt mode. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

'0' (default) - The **EVENT** pin will function in comparator mode

'1' - The **EVENT** pin will function in interrupt mode

Table 7.4 TS Configuration Register

ADDR	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
01	R/W	RFU	RFU	RFU	RFU	RFU	HYST[1:0]		SHDN	0000
		TCRIT_LOCK	EVENT_LOCK	CLEAR	EVENT_STS	EVENT_CTRL	TCRIT_ONLY	EVENT_POL	EVENT_MODE	

Table 7.5 HYST Bit Decode

HYST[1:0]		HYSTERESIS
1	0	
0	0	Disable Hysteresis (Default)
0	1	1.5°C
1	0	3°C
1	1	6°C

7.7 TS Register Value Definitions

Temperatures in the High Limit Register, Low Limit Register, TCRIT Register, and Temperature Data Register are expressed in two's complement format. Bits B12 through B2 for each of these registers are defined for all device resolutions as defined in the TRES field of the Capabilities Register, hence a 0.25 °C minimum granularity is supported in all registers. Examples of valid settings and interpretation of temperature register bits:

The TRES field of the Capabilities Register optionally defines higher resolution devices. For compatibility and simplicity, this additional resolution affects only the Temperature Data Register but none of the Limit Registers. When higher resolution devices generate status or **EVENT** changes, only bits B12 through B2 are used in the comparison; however, all 11 bits (TRES[1-0] = 10) or all 12 bits (TRES[1-0] = 11) are visible in reads from the Temperature Data Register.

When a lower resolution device is indicated in the Capabilities Register (TRES[1-0] = 00), the finest resolution supported is 0.5 °C. When this is detected, bit 2 of all Limit Registers should be programmed to 0 to assure correct operation of the temperature comparators.

Table 7.6 Temperature Register Coding Examples

B15~B0 (Binary)	Value	Units
XXX0 0000 0010 11xx	+2.75	°C
XXX0 0000 0001 00xx	+1.00	°C
XXX0 0000 0000 01xx	+0.25	°C
XXX0 0000 0000 00xx	0	°C
XXX1 1111 1111 11xx	-0.25	°C

XXX1 1111 1111 00xx	-1.00	°C
XXX1 1111 1101 01xx	-2.75	°C

7.8 TS High Limit Register

The temperature limit registers (High, Low, and TCRIT) define the temperatures to be used by various on chip comparators to determine device temperature status and thermal EVENTs. For future compatibility, unused bits "-" must be programmed as 0.

The High Limit Register holds the High Limit for the nominal operating window. When the temperature rises above the High Limit, or drops below or equal to the High Limit, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register see Table 7.4), then this register becomes read-only.

Table 7.7 High Limit Register

ADDR	R/$\overline{W}$	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
02	R/$\overline{W}$	-	-	-	Sign	128	64	32	16	
		8	4	2	1	0.5	0.25	-	-	

7.9 TS Low Limit Register

The Low Limit Register holds the lower limit for the nominal operating window. When the temperature drops below the Low Limit or rises up to meet or exceed the Low Limit, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register see Table 7.4), then this register becomes read-only.

Table 7.8 Low Limit Register

ADDR	R/$\overline{W}$	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
03	R/$\overline{W}$	-	-	-	Sign	128	64	32	16	
		8	4	2	1	0.5	0.25	-	-	

7.10 TCRIT Limit Register

The TCRIT Limit Register holds the TCRIT Limit. If the temperature exceeds the limit, the $\overline{\text{EVENT}}$ pin will be asserted. It will remain asserted until the temperature drops below or equal to the limit minus hysteresis. If the TCRIT_LOCK bit is set in the Configuration Register (see Table 7.4), then this register becomes read-only.

Table 7.9 TCRIT Limit Register

ADDR	R/$\overline{W}$	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
04	R/$\overline{W}$	-	-	-	Sign	128	64	32	16	
		8	4	2	1	0.5	0.25	-	-	

7.11 Temperature Data Register

The Temperature Data Register holds the 10-bit + sign data for the internal temperature measurement as well as the status bits indicating which error conditions, if any, are active. The encoding of bits B12 through B0 is the same as for the temperature limit registers.

Bit15 - TCRIT -- When set, the temperature is above the TCRIT Limit. This bit will remain set so long as the temperature is above TCRIT and will automatically clear

once the temperature has dropped below the limit minus the hysteresis.

Bit14 - HIGH -- When set, the temperature is above the High Limit. This bit will remain set so long as the temperature is above the HIGH limit. Once set, it will only be cleared when the temperature drops below or equal to the HIGH Limit minus the hysteresis.

Bit13 - LOW -- When set, the temperature is below the Low Limit. This bit will remain set so long as the temperature is below the Low Limit minus the hysteresis. Once set, it will only be cleared when the temperature meets or exceeds the Low Limit

Table 7.10 Temperature Data Register

ADDR	R/$\overline{W}$	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
05	R	TCRIT	HIGH	LOW	Sign	128	64	32	16	N/A(0000)
		8	4	2	1	0.5	0.25*	0.125*	0.0625*	

Note: * Resolution defined based on value of TRES field of the Capabilities Register. Unused/unsupported bits will read as 0.

7.12 Manufacture ID Register

The Manufacturer ID Register holds the PCI SIG number assigned to the specific manufacturer. This register is not available on EE1004-v devices.

Table 7.11 TSE Manufacture ID Register

ADDR	R/$\overline{W}$	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
06	R	0	0	0	1	1	1	0	0	1C68
		0	1	0	0	1	0	0	0	

7.13 Device ID / Revision Register

The upper byte of the Device ID / Revision Register must be 0x22 for the GT34TS04A. The lower byte holds the revision value which is vendor-specific. This register is not available on EE1004-v devices.

Table 7.12 TSE Device ID/Revision Register

ADDR	R/$\overline{W}$	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
07	R	0	0	1	0	0	0	1	0	2202
		0	0	0	0	0	0	0	1	

7.14 SMBus Timeout Register

The SMBus Register allows the user to enable or disable the SMBus time out feature

Bits15 - 8 -- RFU - Reserved for future use. These bits will always read ‘0’ and writing to them will have no effect.

Bit7 - SMBOUT -- When the SMBOUT is set to ‘0’ , the SMBus Timeout function is enable. If the SMBOUT is set to ‘1’, the SMBus Timeout is disable.

Bits6 - 0 -- RFU - Reserved for future use. These bits will always read ‘0’ and writing to them will have no effect.

This bit can be set when Temperature Sensor enter shutdown mode.

When either of the Crit_Alarm Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.

ADDR	R/$\overline{W}$	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
08	R/$\overline{W}$	0	0	0	0	0	0	0	0	0000
		SMBOUT	0	0	0	0	0	0	0	

Table 7.14 Temperature Resolution Register

7.15 Temperature Resolution Register

With this register a user can program the temperature sensor resolution from 9-12 bits as shown below. The power-on default is always 10 bit (0.25 °C/LSB). The selected resolution RES[1:0] is also reflected in bits (4:3) (TRES1:TRES0) of the capability register.

Table 7.15 Temperature Resolution Register

ADDR	R/$\overline{W}$	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default
09	R/$\overline{W}$	0	0	0	0	0	0	0	0	0001
		0	0	0	0	0	0	RES[1:0]		

Note: In order to prevent accidentally writing the resolution register to higher resolution and exceeding the maximum temperature conversion time of tCONV = 125 ms, a Shutdown Command (using the CONFIG register) is required to change the resolution register. The device must be in shutdown mode to change the resolution.

Table 7.16 Resolution Bit Decode

RES[1:0]		Temperature Resolution
0	0	0.5°C (9-bit)
0	1	0.25°C (10-bit)
1	0	0.125°C (11-bit)
1	1	0.0625°C (12-bit)

Figure 7.1 TS Register Write Operation

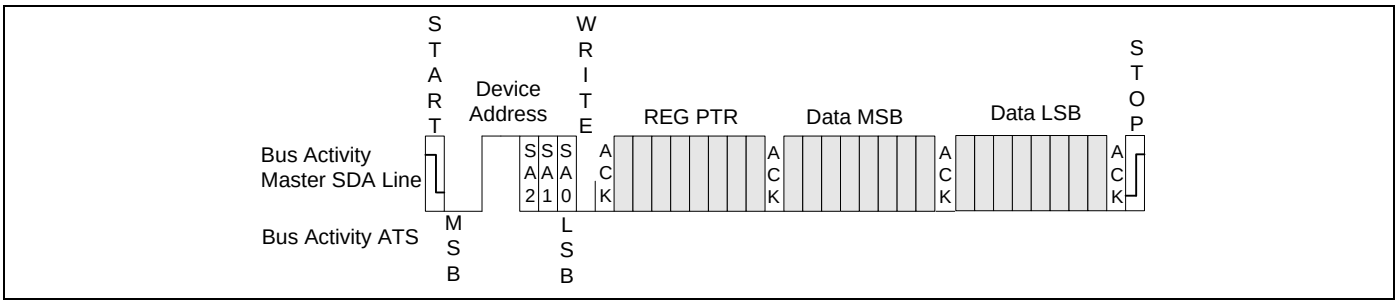


Figure 7.2 I²C Bus Write to Pointer Register

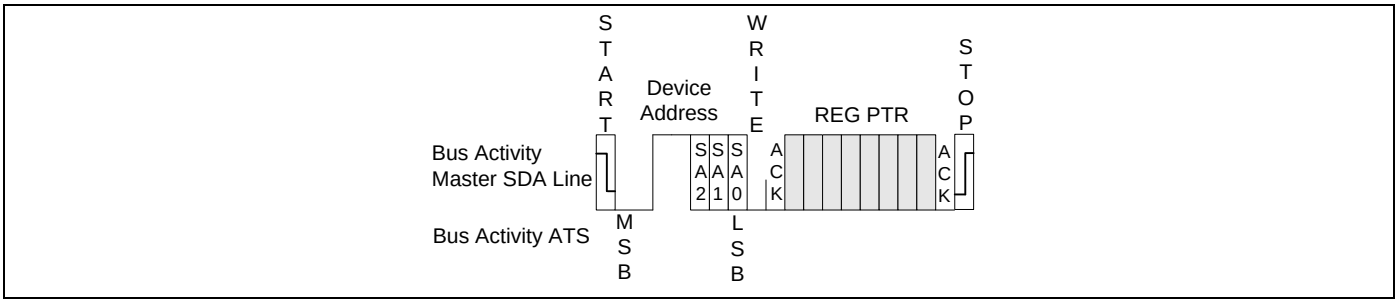


Figure 7.3 I²C Bus Preset Pointer Register Word Read

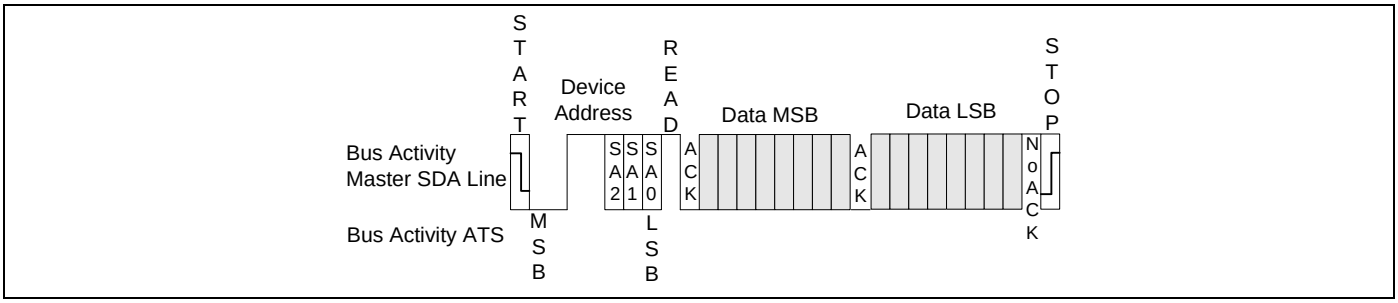


Figure 7.4 I²C Bus Pointer Write Register Word Read

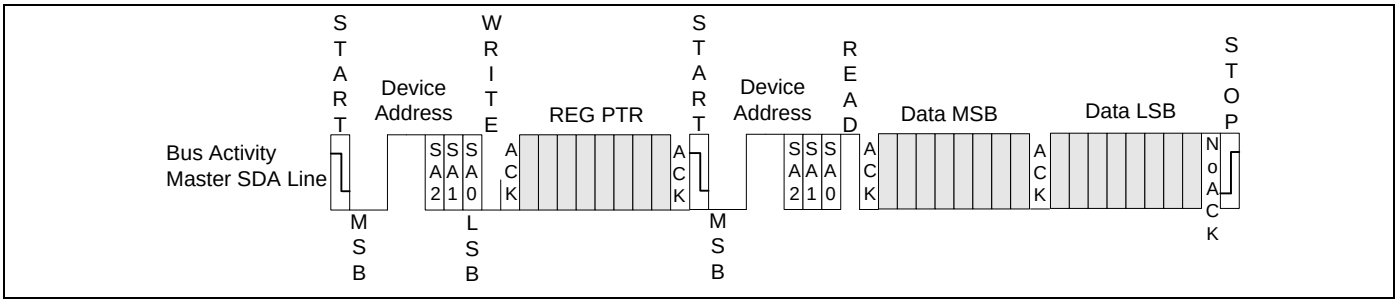
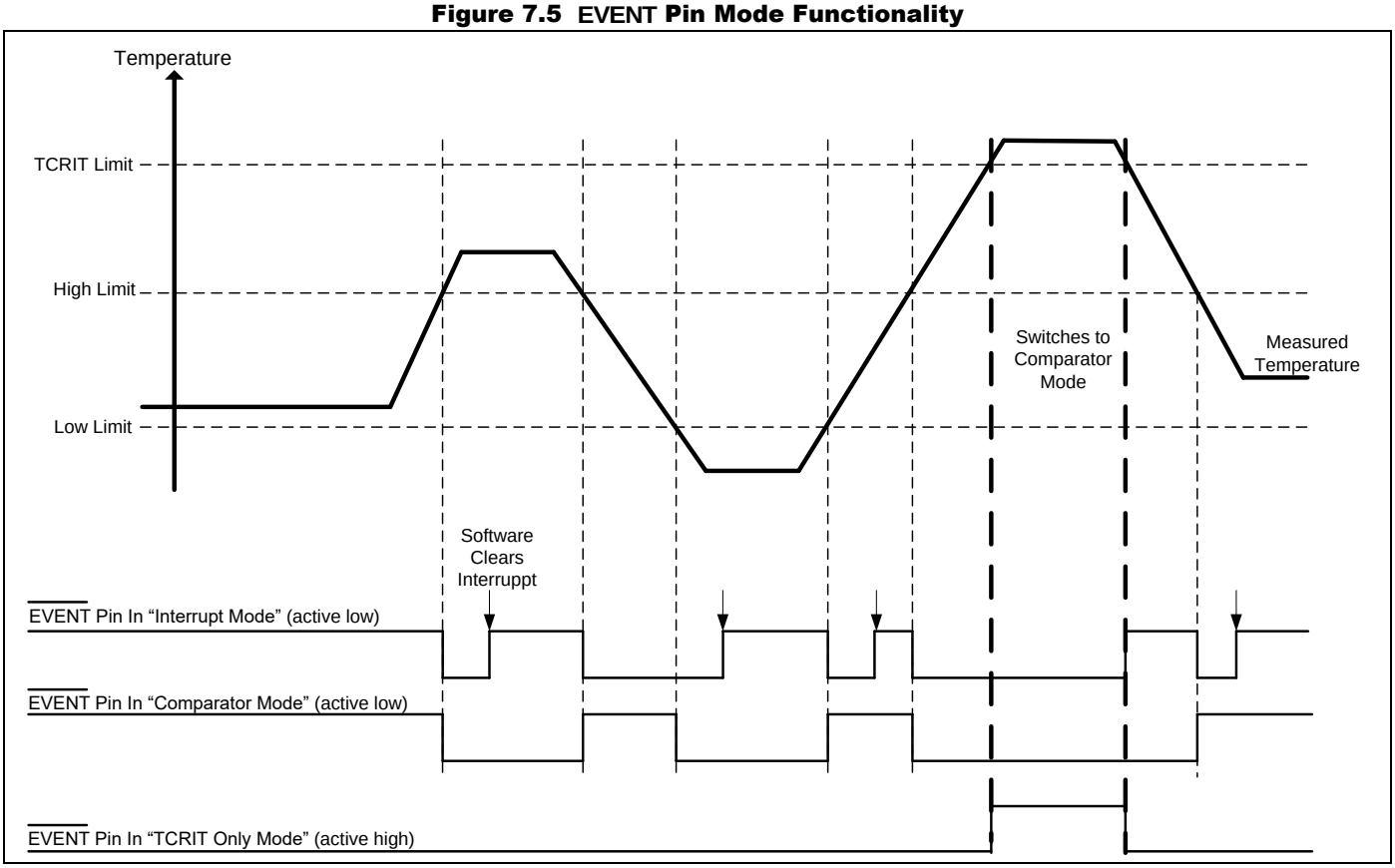


Figure 7.5 $\overline{\text{EVENT}}$ Pin Mode Functionality



8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 4.3	V
V_N	Voltage on SDA, SCL and $\overline{\text{EVENT}}$ Pins	–0.5 to + 4.3	V
V_{SA0}	Voltage on pin SA0	-0.5 to +10	V
$T_{J(max)}$	Maximum Junction Temperature	150	°C
T_{stg}	Storage Temperature	–65 to +150	°C

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	-40°C to +125°C	1.7V to 3.6V

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

8.3 Capacitance

Symbol	Parameter[1, 2]	Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	--	--	6	pF
$C_{I/O}$	Input / Output Capacitance	--	--	8	pF
Z_{EIL}	Ei (SA0, SA1, SA2) input impedance	V_{IN}<0.3*V_{CC}	30	--	KΩ
Z_{EIH}	Ei (SA0, SA1, SA2) input impedance	V_{IN}>0.7*V_{CC}	800	--	KΩ
T_{SP}	Pulse width of spikes which must be suppressed by the input filter	Single glitch, f≤100KHz	--	--	ns
		Single glitch, f≥100KHz	0	50	

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

[2] Test conditions: T_A = 25°C, f = 400 KHz, V_{CC} = 1.7V to 3.6V, unless otherwise specified.

8.4 AC Measurement Conditions

Symbol	Parameter	Min	Max	Units
C_L	Load capacitance	100		pF
	Input rise and fall times	--	50	ns
	Input levels	0.2*V_{CC} to 0.8*V_{CC}		V
	Input and output timing reference levels	0.3*V_{CC} to 0.7*V_{CC}		V

8.5 DC Electrical Characteristic

V_{CC} = 1.7V to 3.6V, T_{amb} = -40 °C to +85 °C, unless otherwise specified

Symbol	Parameter[1]	Conditions	f≤400KHz		F≥400KHz		Unit
			Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage current(SCL, SDA)	V_{IN}=V_{CC} or GND	--	±5	--	±5	μA
I_{LO}	Output leakage current	V_{OUT}=V_{CC} or GND, SDA in Hi-Z	--	±5	--	±5	μA
I_{SB1}	Shut down current	TS shutdown , EE standby	--	5	--	5	μA
I_{SB2}	Standby supply current	TS active, EE standby	--	500	--	500	μA
I_{CC}	Supply current	TS shutdown and EE active	--	2	--	2	mA
V_{IH}	Input High Voltage	SCL, SDA	0.7* V_{CC}	V_{CC}+0.5	0.7* V_{CC}	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	SCL, SDA	-0.5	0.3* V_{CC}	-0.5	0.3* V_{CC}	V
V_{HV}	SA0 High Voltage	V_{HV} - V_{CC} ≥ 4.8V	7	10	7	10	V
V_{OL1}	Output Low Voltage [2] open-drain or open-collector	I_{OL}=3mA, V_{CC}>2.2V	--	0.4	--	0.4	V
V_{OL2}		I_{OL}=2mA, V_{CC}≤2.2V	--	0.2	--	0.2	
I_{OL}	Output Low Sink Current[3]	V_{OL}=0.4V	3		20		mA
		V_{OL}=0.6V	6		--		mA
V_{HYST}	Input hysteresis	V_{CC}<2V	0.10*V_{CC}	--	0.10*V_{CC}	--	V
		V_{CC}≥2V	0.05*V_{CC}	--	0.05*V_{CC}	--	V
V_{PON}	Power On Reset threshold	Monotonic rise between V_{PON} and V_{CC}(min) without ringback	1.6	--	1.6	--	V
V_{POFF}	Power Off threshold for warm power on cycle	No ringback above V_{POFF}	--	0.9	--	0.9	V

Notes: [1] The parameters are characterized but not 100% tested.

[2] The same resistor value to drive 3mA at 3.0V, V_{CC} provides the same RC time constant when using<2V, V_{CC} with a smaller current draw

[3] In order to drive full bus load at 400KHz, 6mA IOL is required at 0.6V VOL. Parts not meeting this specification can still function, but not at 400KHz and 400pF.

8.6 AC Electrical Characteristic

V_{CC} = 1.7V to 3.6V, T_{amb} = 25°C, unless otherwise specified

Symbol	Parameter [11]	V_{CC}[4]<2.2V		V_{CC}≥2.2V				Unit
		100KHz[10]		400KHz[9]		1000KHz		
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	10	100	10	400	10	1000	kHz
T_{LOW}[6]	Low period of SCL clock	4700		1300		500		ns
T_{HIGH}	High period of SCL clock	4000		600		260		ns
T_{BUF}	Bus free time between a Stop and a Start conditions	4700		1300		500		ns
$T_{SU;STA}$[1]	Start condition Setup time	4700		600		260		ns
$T_{HD;STA}$	Start condition Hold time	4000		600		260		ns
$T_{SU;STO}$	Stop condition Setup time	4000		600		260		ns
$T_{SU;DAT}$	Data In Setup time	250		100		50		ns
$T_{HD;DI}$ [2]	Data In Hold time	0		0		0		ns
$T_{HD:DAT}$	Data Out Hold Time	200	3450	200	900	0	350	ns
T_W	Write Cycle		5		5		5	ms
T_R[2]	Rise time of SDA	--	1000	20	300	--	120	ns
T_F[2]	Fall time of SDA	--	300	20	300	--	120	ns
T_{INIT}	Time from power on to first command	10		10		10		ns
T_{POFF}	Warm power cycle off time	1		1		1		ms
$T_{time\text{-}out}$ [5,7]	Detect clock low timeout	25	35	25	35	25	35	ms

Notes: [1] For a reSTART condition, or following a write cycle.

[2] Guaranteed by design and characterization, not necessarily tested.

[3] To avoid spurious START and STOP conditions, a minimum delay is placed between falling edge of SCL and the falling or rising edge of SDA.

[4] VDDSPD below 2.2 V only supported on EE1004-1 and TSE2004a1, not on EE1004-2 or TSE2004a2.

[5] Unlike previous EE generations, EE1004-v and TSE2004av families must support bus timeout on EE accesses.

[6] EE1004-v and TSE2004av family devices shall not initiate clock stretching, which is an optional I2C Bus feature.

[7] I2C bus masters can terminate a transaction in process and reset device communication on the bus by asserting SCL low for $T_{TIMEOUT}$,MAX or longer. EE/TSE devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $T_{TIMEOUT}$,MAX. EE/TSE devices will not reset if SCL stretching is less than $T_{TIMEOUT}$, MIN. See EE/TSE Bus Timeout Waveforms.

[8] EE/TSE devices are not required to support the I2C Bus ALERT function.

[9] 400 KHz timing defined for compatibility with EE1002(A) and TSE2002av applications.

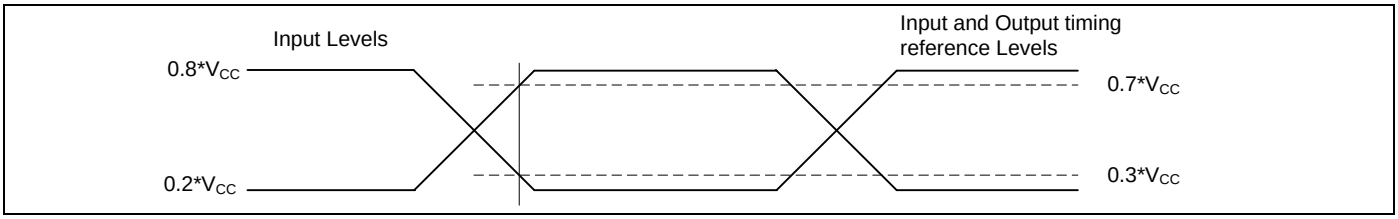
[10] 100 KHz timing compliant with SMBus 2.0 specifications.

[6] Not all parameters are 100% tested .

8.7 Temperature to Digital Conversion Performance

Symbol	Parameter [1]	Min.	Typ.	Max.	Unit
TS_{Acc}	Temperature sensor (TS) accuracy (B-grade)	T_{amb}= 70 °C to 95 °C	±0.5	±1.0	°C
		T_{amb}= 40 °C to 125 °C	±1.0	±2.0	°C
		T_{amb}= -40 °C to 125 °C	±2.0	±3.0	°C
TS_{Res}	TS Resolution	10-bit ADC		0.25	°C/LSB
R_{ADC}	ADC Resolution			10	Bits
TS_{Conv}	Conversion Rate			125	ms

Figure 8.1 AC Measurement I/O Waveform



9. Ordering Information

Industrial Grade: -40°C to +85°C, Lead-free

Voltage Range	Part Number*	Package (8-pin)*
1.7V to 3.6V	GT34TS04A-2UDLI-TR	2 x 3 x 0.55 mm Ultra-thin DFN

*

1. Contact Giantec Sales Representatives for availability and other package information.
2. The listed part numbers are packed in tape and reel “-TR”. UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

10. Top Markings

10.1 UDFN Package

GT: Giantec Logo

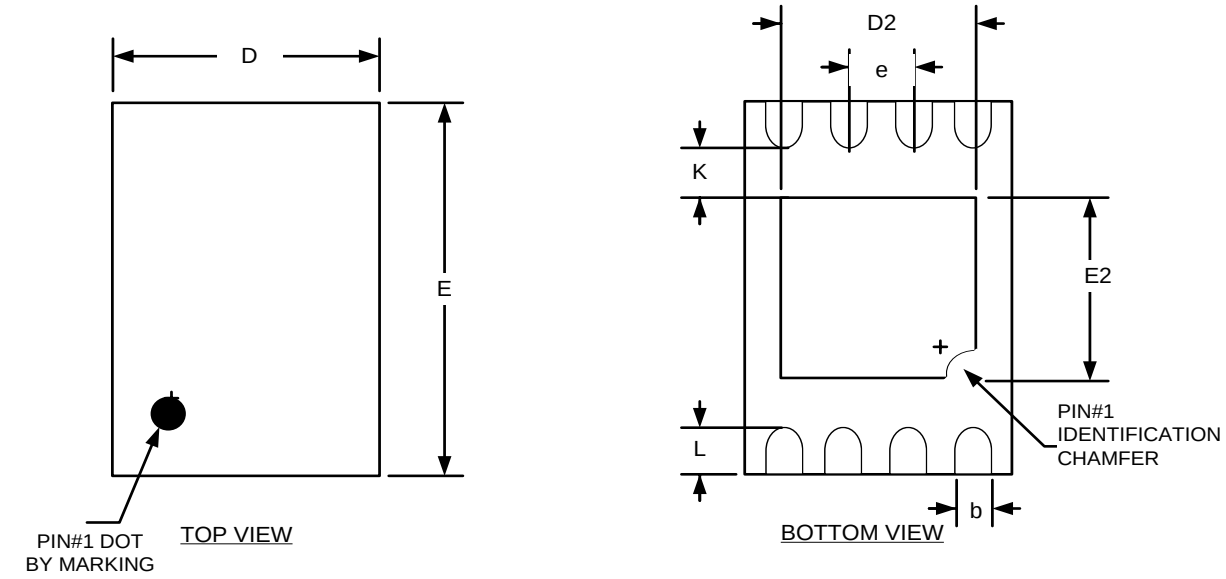
82A: GT34TS04A-2UDLI-TR

YWW: Date Code, Y=year, WW=week

11. Package Information

11.1 UDFN

8L 2x3mm UDFN Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

12. Revision History

Revision	Date	Descriptions
A0	Jan. 2016	Initial version
A0.1	Apr. 2016	Remove I_{SB3}
A1.0	Jan.2017	Remove 0xA~0xFF TS register
A1.1	Oct.2018	Fix incorrect description of temperature and table 8.5
A1.2	Nov.2018	Correct ‘TS Active mode’ to ‘TS Shutdown mode’ in 2mA description.
A2	Oct.2019	Update Set page command response from ‘NACK’ to ‘ACK’
A3	Sep. 2022	Update Logo and other